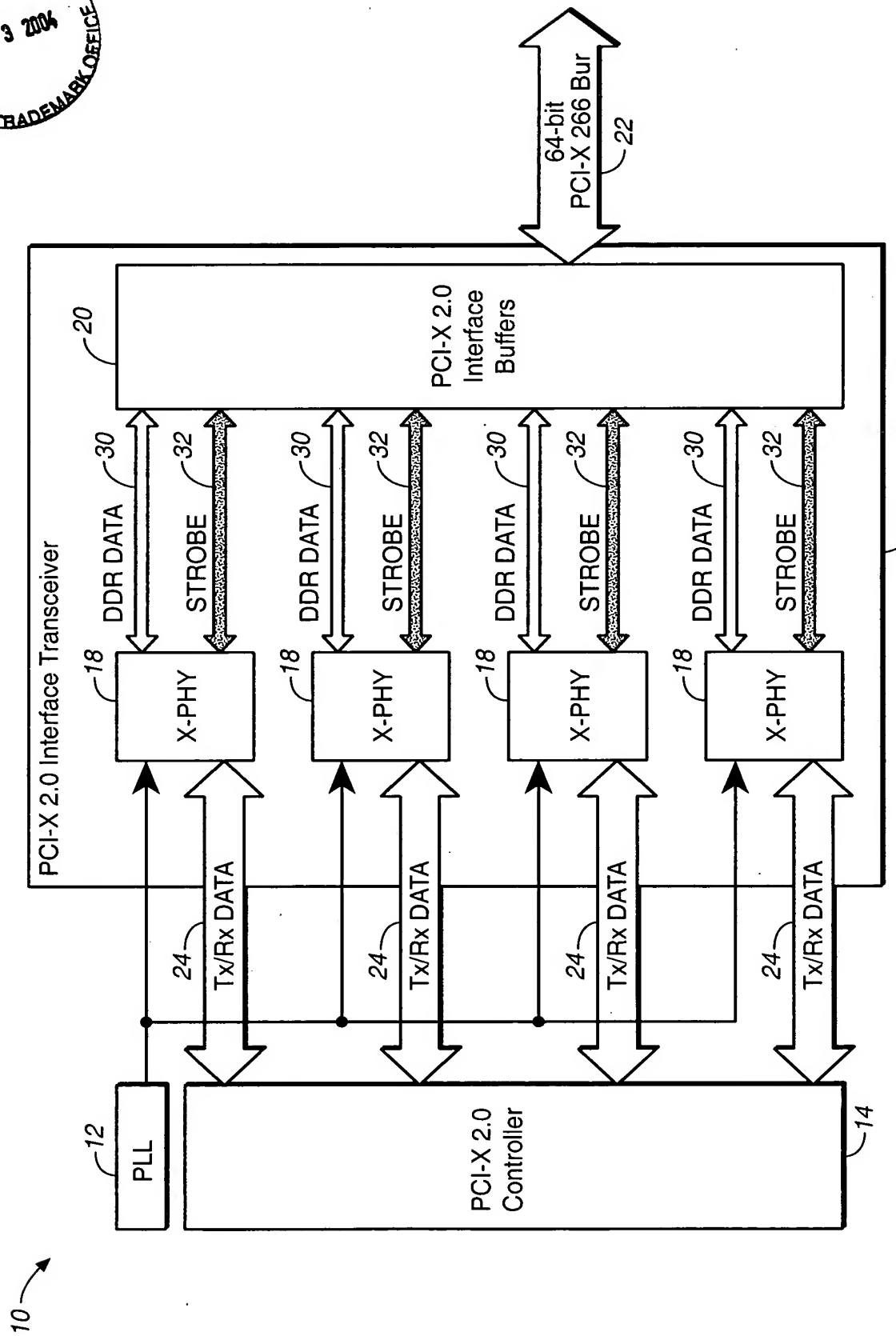


FIG._1

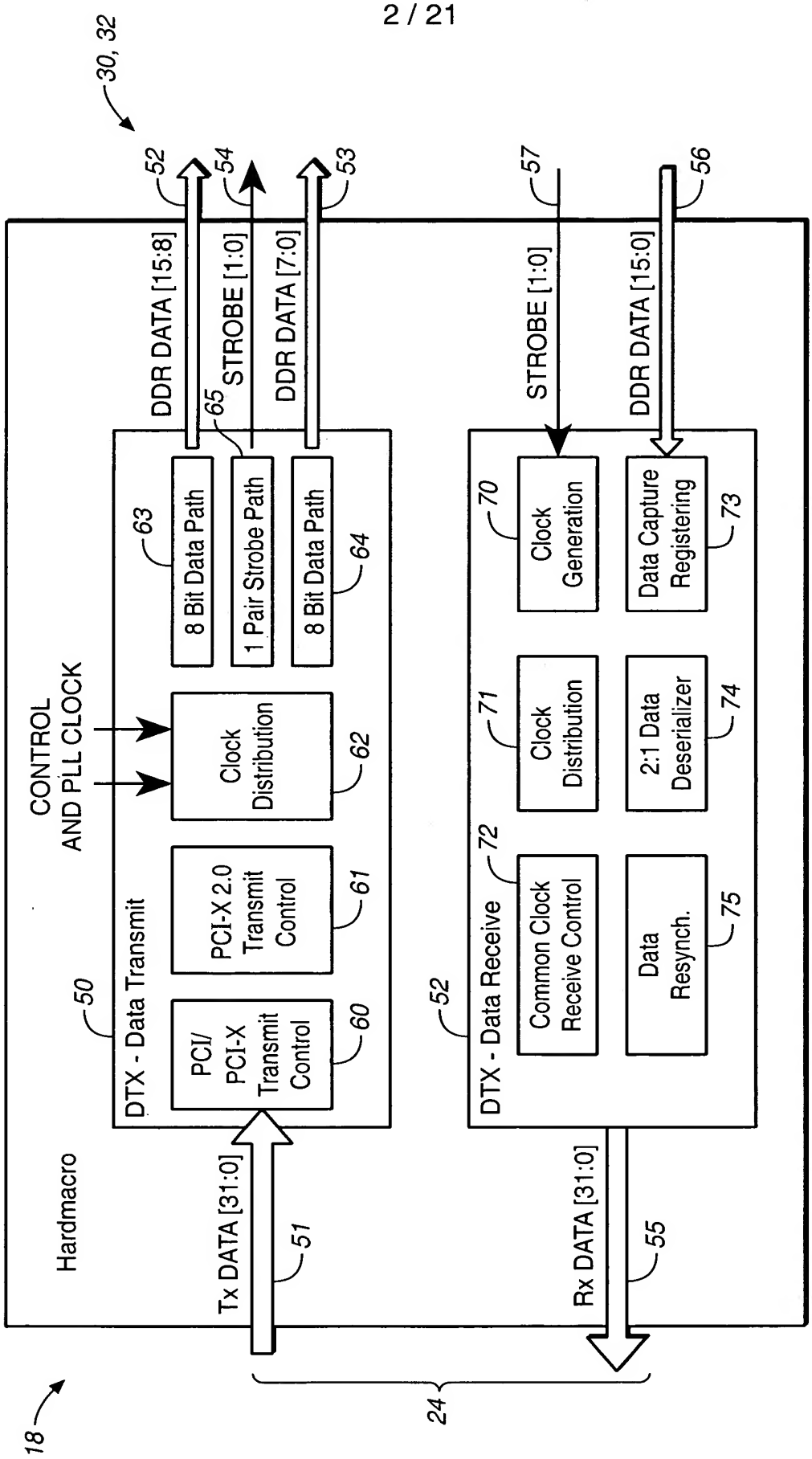

30, 32
52
54
53
57
56
DDR DATA [15:8]
STROBE [1:0]
DDR DATA [7:0]
STROBE [1:0]
DDR DATA [15:0]
65
63
64
70
73
8 Bit Data Path
1 Pair Strobe Path
8 Bit Data Path
Clock Generation
Data Capture Registering
CONTROL AND PLL CLOCK
Clock Distribution
62
71
74
Clock Distribution
2:1 Data Deserializer
PCI-X 2.0 Transmit Control
61
72
75
Common Clock Receive Control
Data Resynch.
50
52
PCI/ PCI-X Transmit Control
60
DTX - Data Transmit
DTX - Data Receive
Hardmacro
Tx DATA [31:0]
51
Rx DATA [31:0]
55
24
18

FIG._2

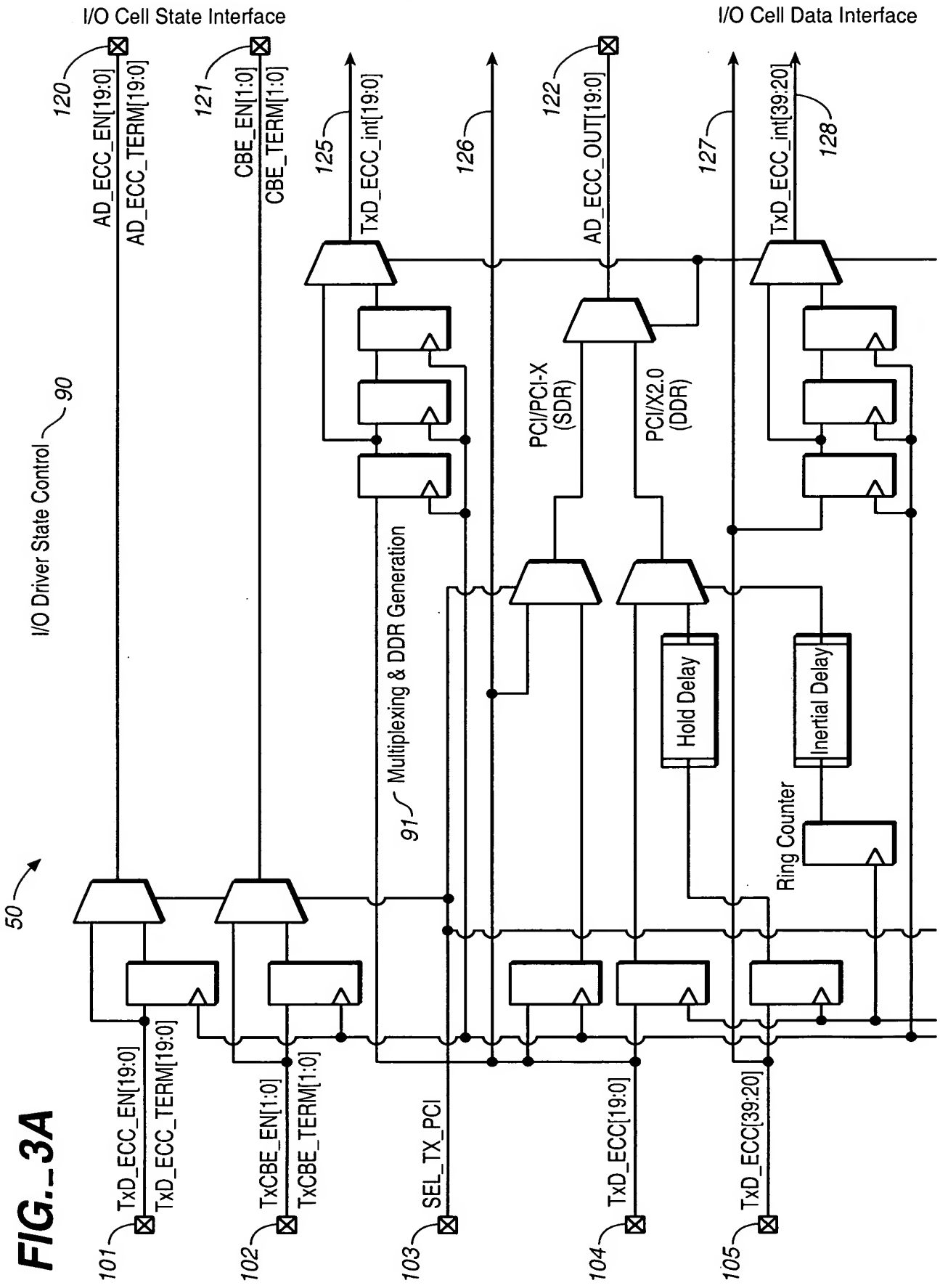

I/O Cell State Interface
I/O Cell Data Interface
I/O Driver State Control
90
50
120
AD_ECC_EN[19:0]
AD_ECC_TERM[19:0]
121
CBE_EN[1:0]
CBE_TERM[1:0]
125
TxD_ECC_int[19:0]
126
122
AD_ECC_OUT[19:0]
127
128
TxD_ECC_int[39:20]
PCI/PCI-X (SDR)
PCI/X2.0 (DDR)
Multiplexing & DDR Generation
91
Hold Delay
Inertial Delay
Ring Counter
TxD_ECC_EN[19:0]
TxD_ECC_TERM[19:0]
TxCBE_EN[1:0]
TxCBE_TERM[1:0]
SEL_TX_PCI
TxD_ECC[19:0]
TxD_ECC[39:20]
101
102
103
104
105

FIG._3A

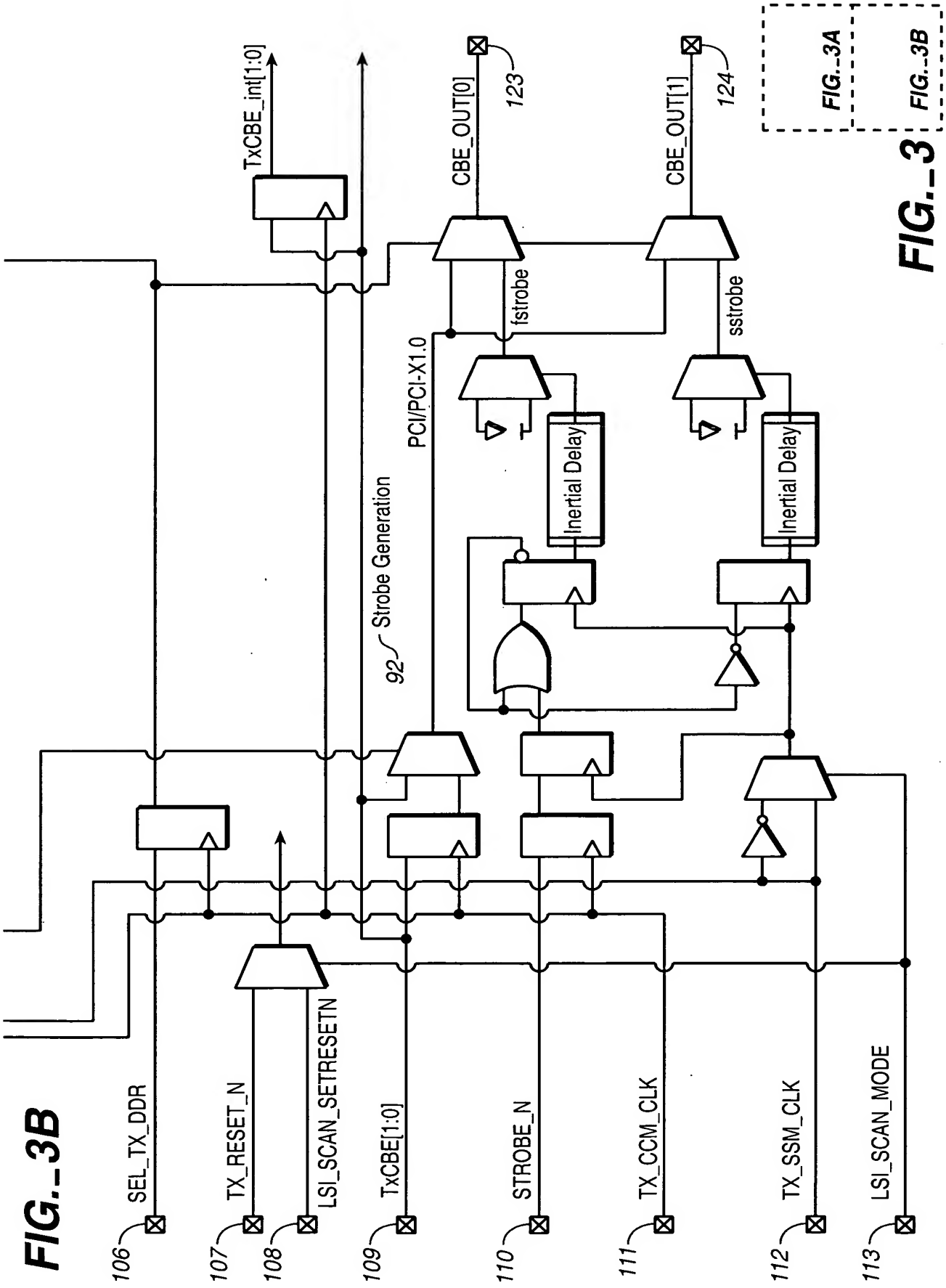

TxCBE_int[1:0]
CBE_OUT[0]
123
CBE_OUT[1]
124
FIG._3A
FIG._3B
fstrobe
sstrobe
PCI/PCI-X1.0
Strobe Generation
92
Inertial Delay
Inertial Delay
SEL_TX_DDR
TX_RESET_N
LSI_SCAN_SETRESETN
TxCBE[1:0]
STROBE_N
TX_CCM_CLK
TX_SSM_CLK
LSI_SCAN_MODE
106
107
108
109
110
111
112
113

FIG._3

FIG._3B

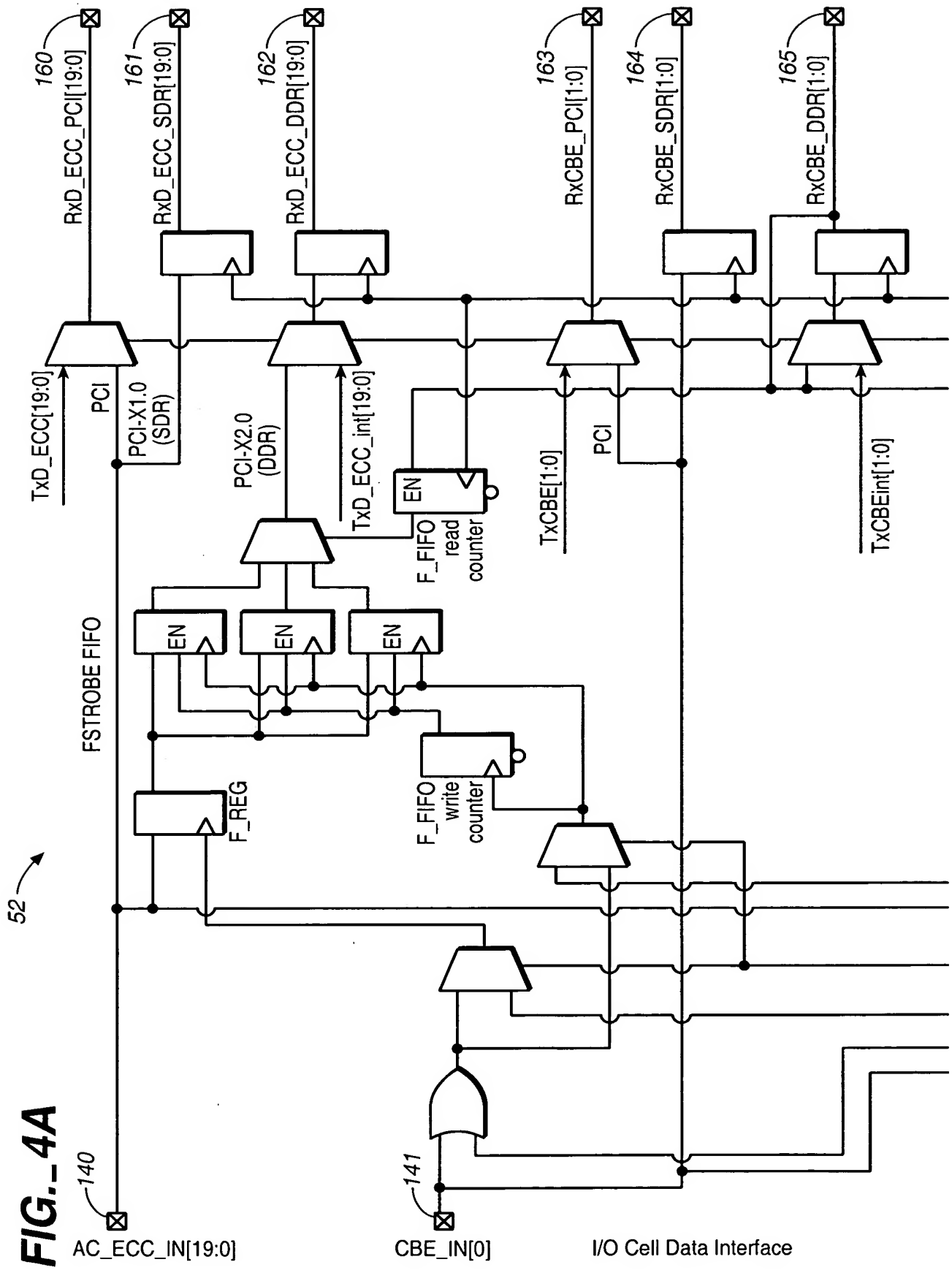

160
RxD_ECC_PCI[19:0]
161
RxD_ECC_SDR[19:0]
162
RxD_ECC_DDR[19:0]
163
RxCBE_PCI[1:0]
164
RxCBE_SDR[1:0]
165
RxCBE_DDR[1:0]
TxD_ECC[19:0]
PCI
PCI-X1.0 (SDR)
PCI-X2.0 (DDR)
TxD_ECC_int[19:0]
EN
F_FIFO read counter
TxCBE[1:0]
PCI
TxCBEint[1:0]
FSTROBE FIFO
EN
EN
EN
F_REG
F_FIFO write counter
52
140
141
AC_ECC_IN[19:0]
CBE_IN[0]
I/O Cell Data Interface

FIG._4A

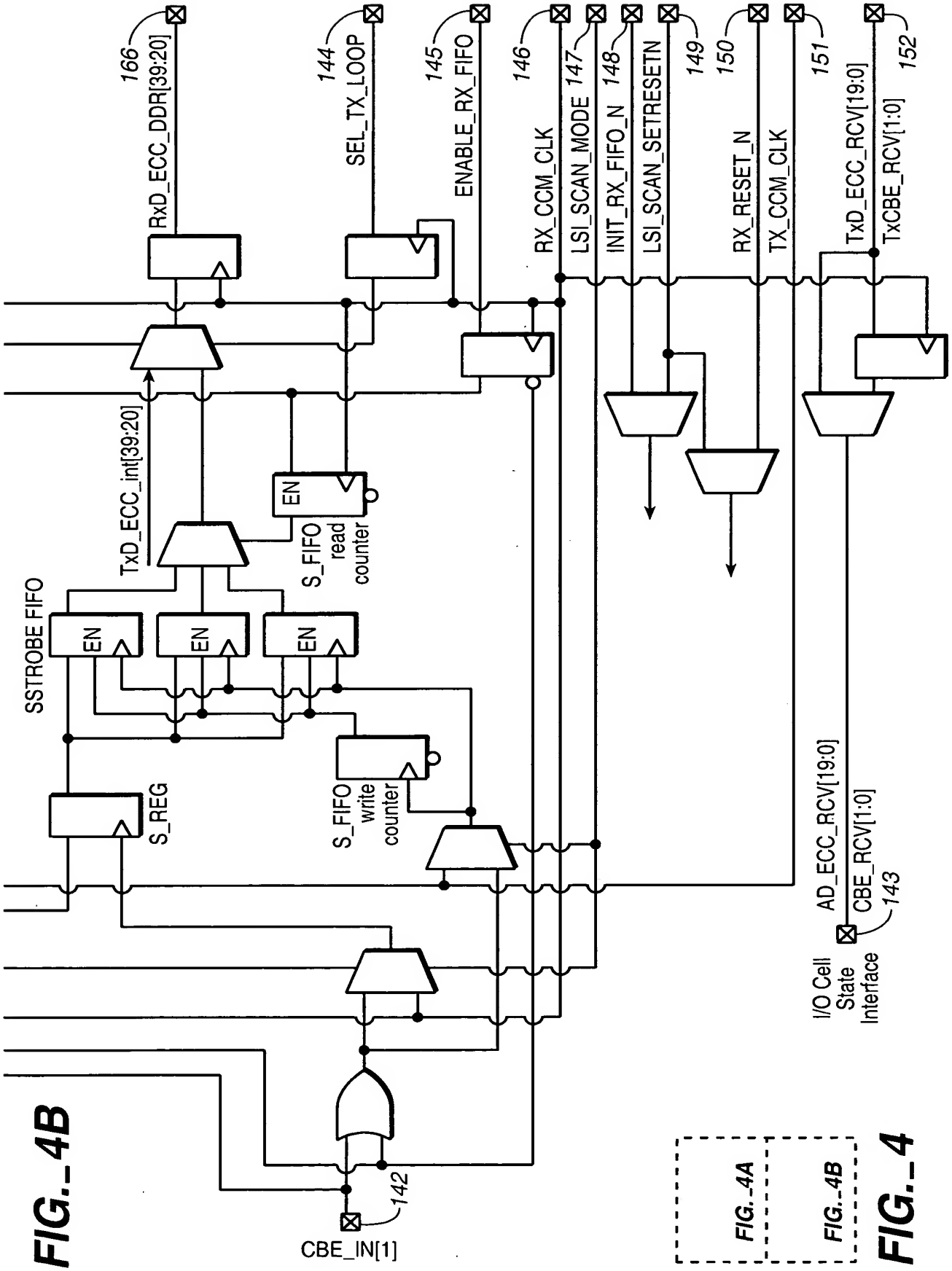


FIG._4B

FIG._4A

FIG._4B

FIG._4

FIG._5

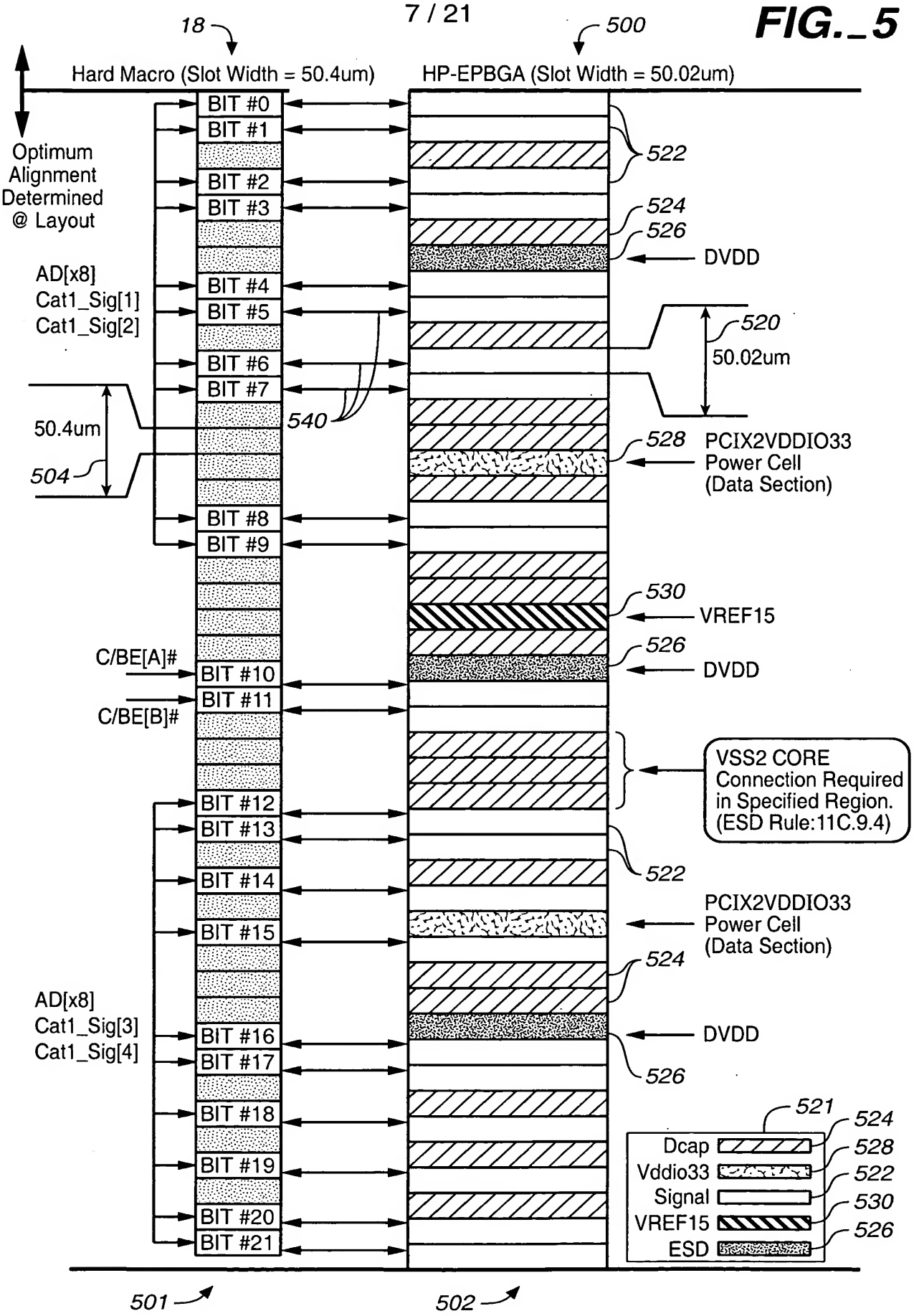

18
500
Hard Macro (Slot Width = 50.4um)
HP-EPBGA (Slot Width = 50.02um)
Optimum Alignment Determined @ Layout
BIT #0
BIT #1
BIT #2
BIT #3
BIT #4
BIT #5
BIT #6
BIT #7
BIT #8
BIT #9
BIT #10
BIT #11
BIT #12
BIT #13
BIT #14
BIT #15
BIT #16
BIT #17
BIT #18
BIT #19
BIT #20
BIT #21
AD[x8] Cat1_Sig[1] Cat1_Sig[2]
AD[x8] Cat1_Sig[3] Cat1_Sig[4]
C/BE[A]#
C/BE[B]#
50.4um
504
540
522
524
526
DVDD
520
50.02um
528
PCIX2VDDIO33 Power Cell (Data Section)
530
VREF15
VSS2 CORE Connection Required in Specified Region. (ESD Rule:11C.9.4)
521
Dcap
Vddio33
Signal
VREF15
ESD
501
502

FIG._6

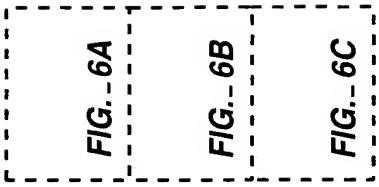


FIG._6A
FIG._6B
FIG._6C

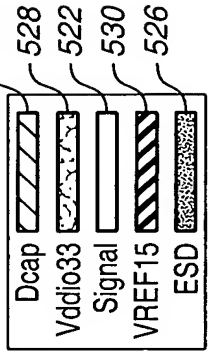
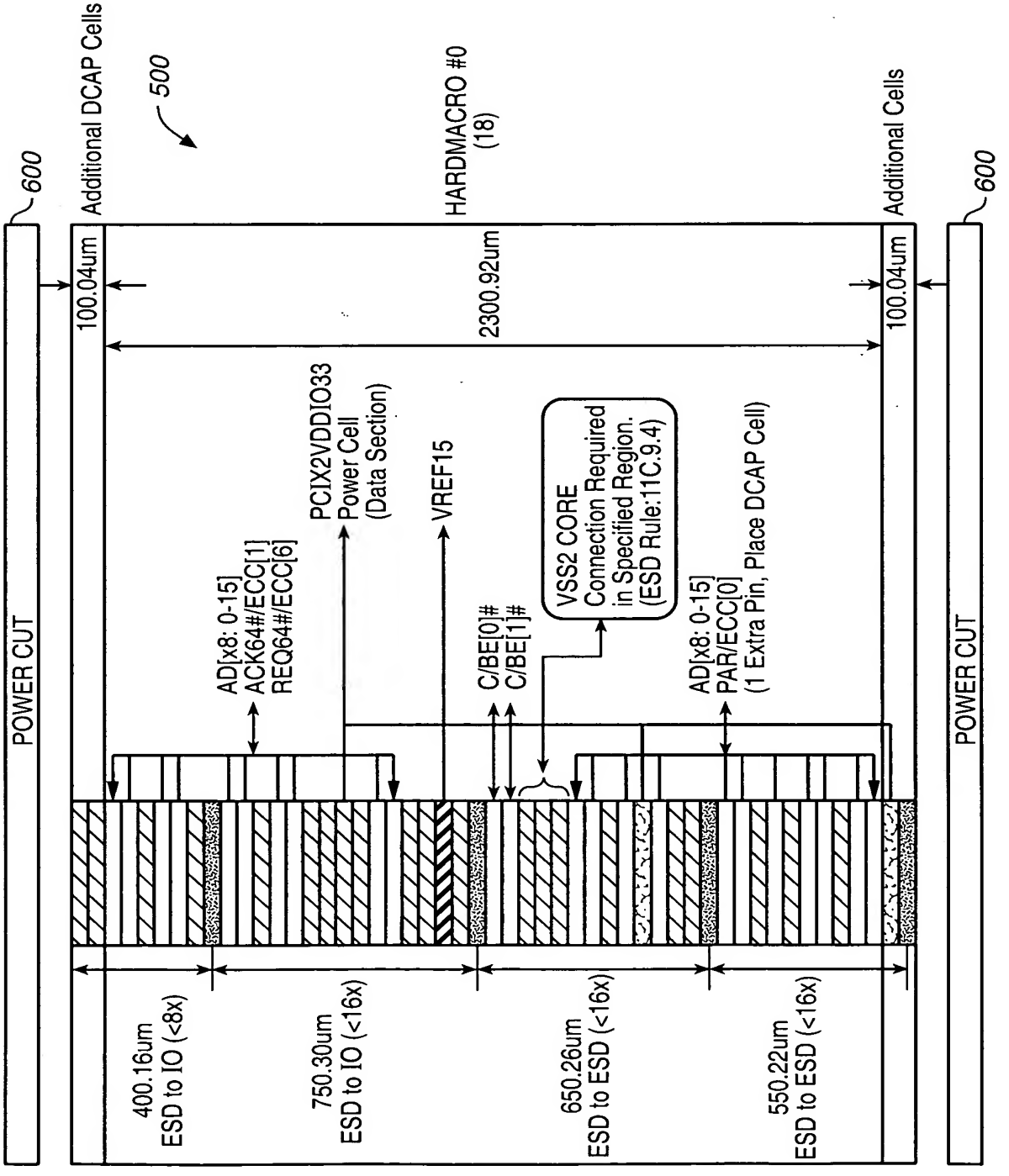

524
528
522
530
526
Dcap
Vddio33
Signal
VREF15
ESD

FIG._6A


600
Additional DCAP Cells
500
HARDMACRO #0
(18)
Additional Cells
600
POWER CUT
100.04um
2300.92um
100.04um
POWER CUT
AD[x8: 0-15]
ACK64#/ECC[1]
REQ64#/ECC[6]
PCIX2VDDIO33
Power Cell
(Data Section)
VREF15
C/BE[0]#
C/BE[1]#
VSS2 CORE
Connection Required
in Specified Region.
(ESD Rule:11C.9.4)
AD[x8: 0-15]
PAR/ECC[0]
(1 Extra Pin, Place DCAP Cell)
400.16um
ESD to IO (<8x)
750.30um
ESD to IO (<16x)
650.26um
ESD to ESD (<16x)
550.22um
ESD to ESD (<16x)

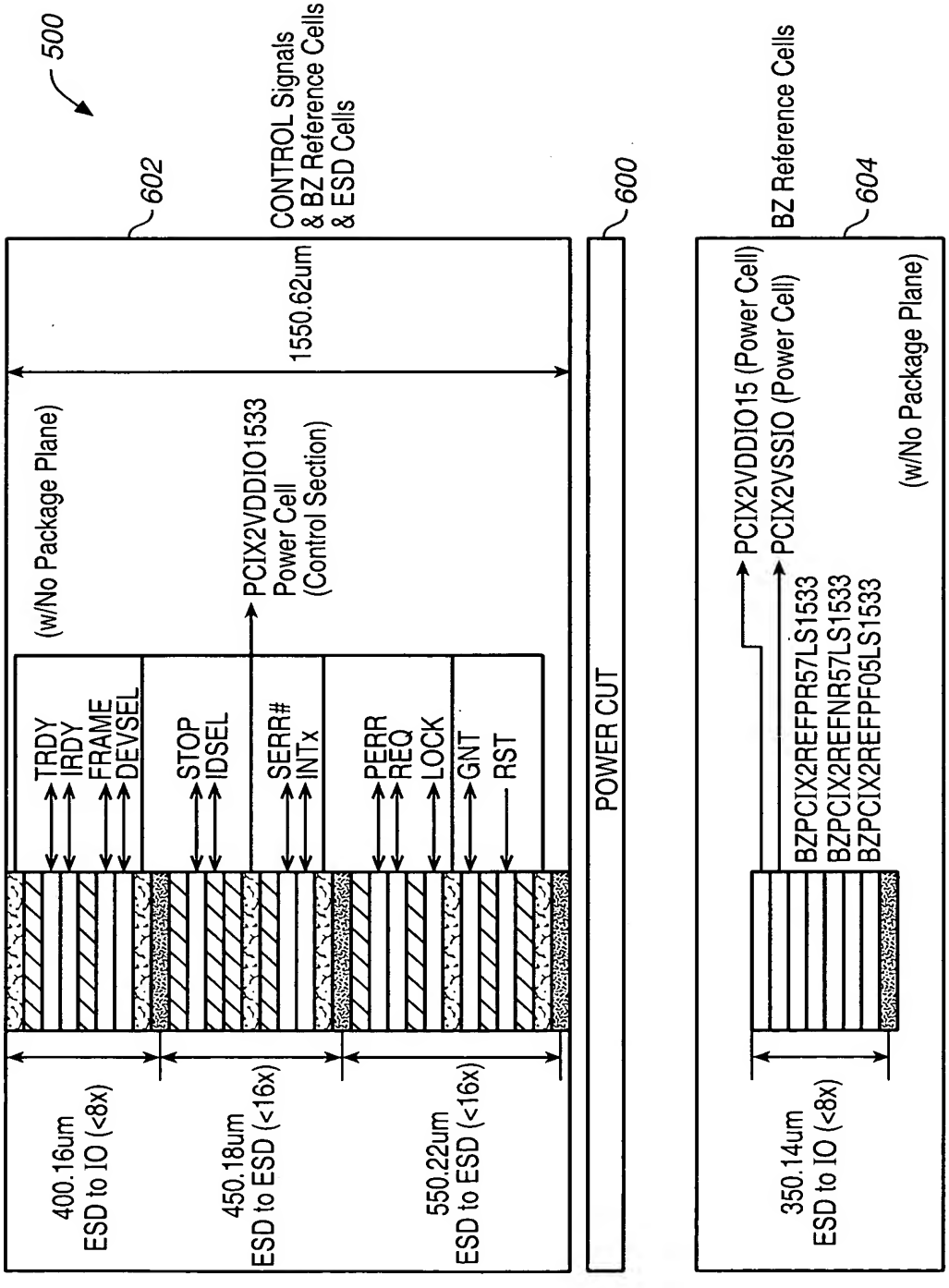

500
602
CONTROL Signals
& BZ Reference Cells
& ESD Cells
1550.62um
(w/No Package Plane)
PCIX2VDDIO1533
Power Cell
(Control Section)
TRDY
IRDY
FRAME
DEVSEL
STOP
IDSEL
SERR#
INTx
PERR
REQ
LOCK
GNT
RST
400.16um
ESD to IO (<8x)
450.18um
ESD to ESD (<16x)
550.22um
ESD to ESD (<16x)
600
POWER CUT
BZ Reference Cells
604
PCIX2VDDIO15 (Power Cell)
PCIX2VSSIO (Power Cell)
BZPCIX2REFPR57LS1533
BZPCIX2REFNR57LS1533
BZPCIX2REFPF05LS1533
(w/No Package Plane)
350.14um
ESD to IO (<8x)

FIG._6B

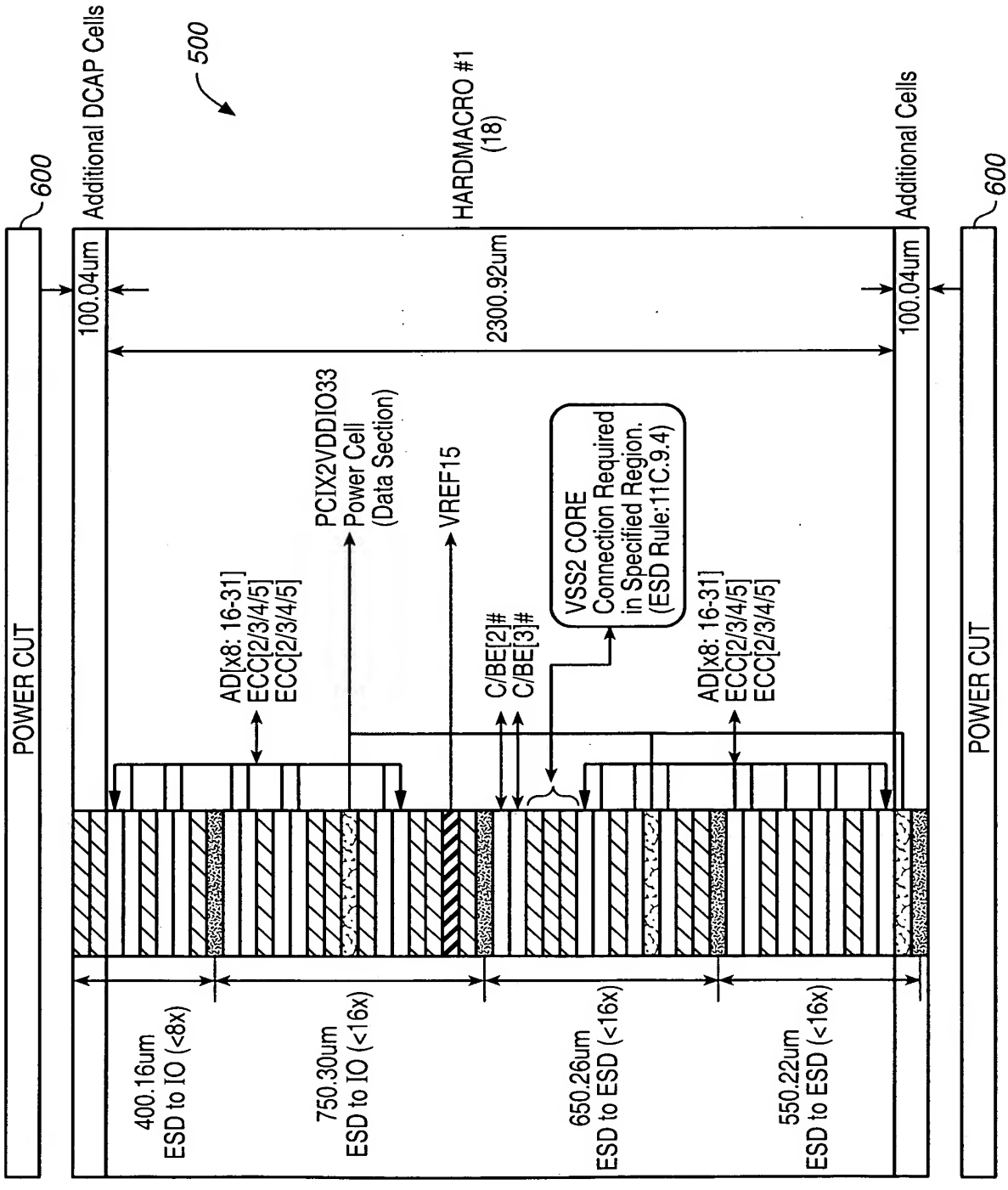

600
Additional DCAP Cells
500
HARDMACRO #1
(18)
Additional Cells
600
POWER CUT
100.04um
2300.92um
100.04um
POWER CUT
PCIX2VDDIO33
Power Cell
(Data Section)
VREF15
VSS2 CORE
Connection Required
in Specified Region.
(ESD Rule:11C.9.4)
AD[x8: 16-31]
ECC[2/3/4/5]
ECC[2/3/4/5]
C/BE[2]#
C/BE[3]#
AD[x8: 16-31]
ECC[2/3/4/5]
ECC[2/3/4/5]
400.16um
ESD to IO (<8x)
750.30um
ESD to IO (<16x)
650.26um
ESD to ESD (<16x)
550.22um
ESD to ESD (<16x)

FIG._6C

FIG._7

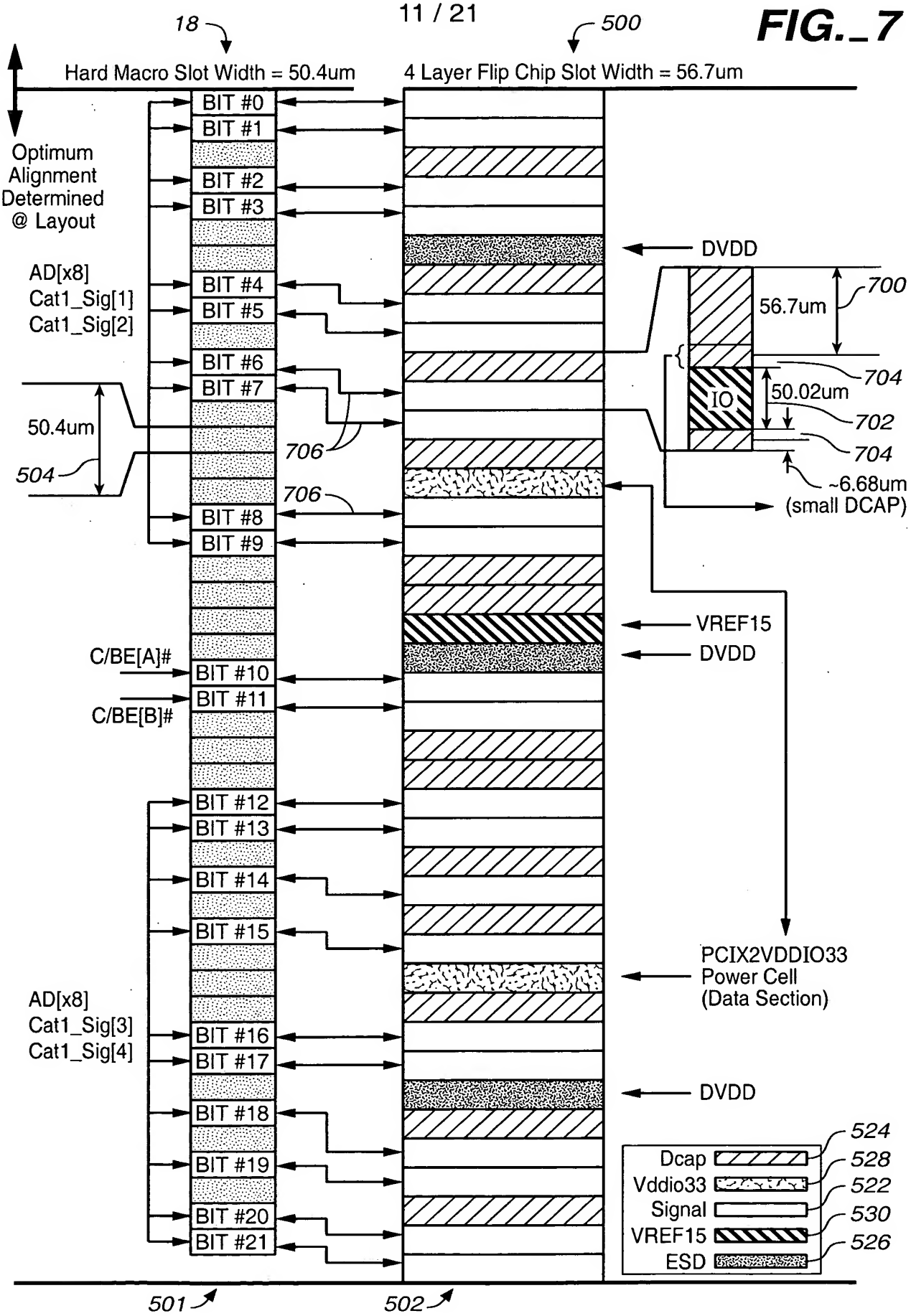

18
500
Hard Macro Slot Width = 50.4um
4 Layer Flip Chip Slot Width = 56.7um
Optimum Alignment Determined @ Layout
AD[x8] Cat1_Sig[1] Cat1_Sig[2]
AD[x8] Cat1_Sig[3] Cat1_Sig[4]
C/BE[A]#
C/BE[B]#
BIT #0
BIT #1
BIT #2
BIT #3
BIT #4
BIT #5
BIT #6
BIT #7
BIT #8
BIT #9
BIT #10
BIT #11
BIT #12
BIT #13
BIT #14
BIT #15
BIT #16
BIT #17
BIT #18
BIT #19
BIT #20
BIT #21
50.4um
504
706
706
DVDD
56.7um
700
704
IO
50.02um
702
704
~6.68um
(small DCAP)
VREF15
DVDD
PCIX2VDDIO33
Power Cell
(Data Section)
DVDD
Dcap
Vddio33
Signal
VREF15
ESD
524
528
522
530
526
501
502

FIG._8

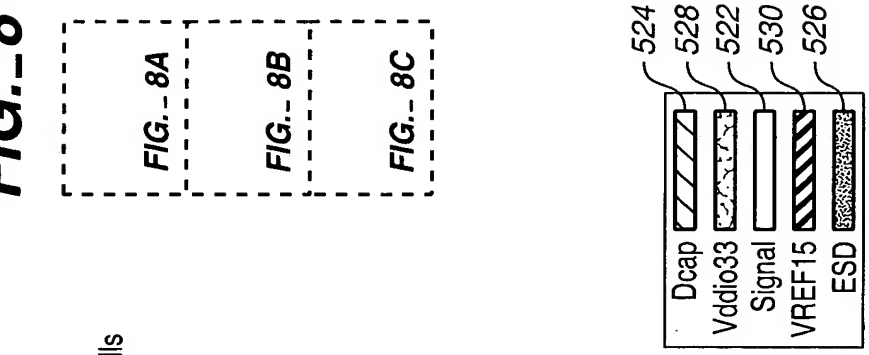


FIG._8A
FIG._8B
FIG._8C

FIG._8A

524
528
522
530
526
Dcap
Vddio33
Signal
VREF15
ESD
500
600
Additional DCAP Cells
HARDMACRO #0
(18)
Additional Cells
POWER CUT
POWER CUT
113.40um
2324.70um
170.10um
AD[x8: 0-15]
ACK64#/ECC[1]
REQ64#/ECC[6]
PCIX2VDDIO33
Power Cell
(Data Section)
VREF15
C/BE[0]#
C/BE[1]#
AD[x8: 0-15]
PAR/ECC[0]
(1 Extra Pin, Place DCA Cell)
396.90um
ESD to IO (<8x)
737.10um
ESD to IO (<16x)
793.80um
ESD to ESD (<16x)
396.90um
ESD to ESD (<16x)

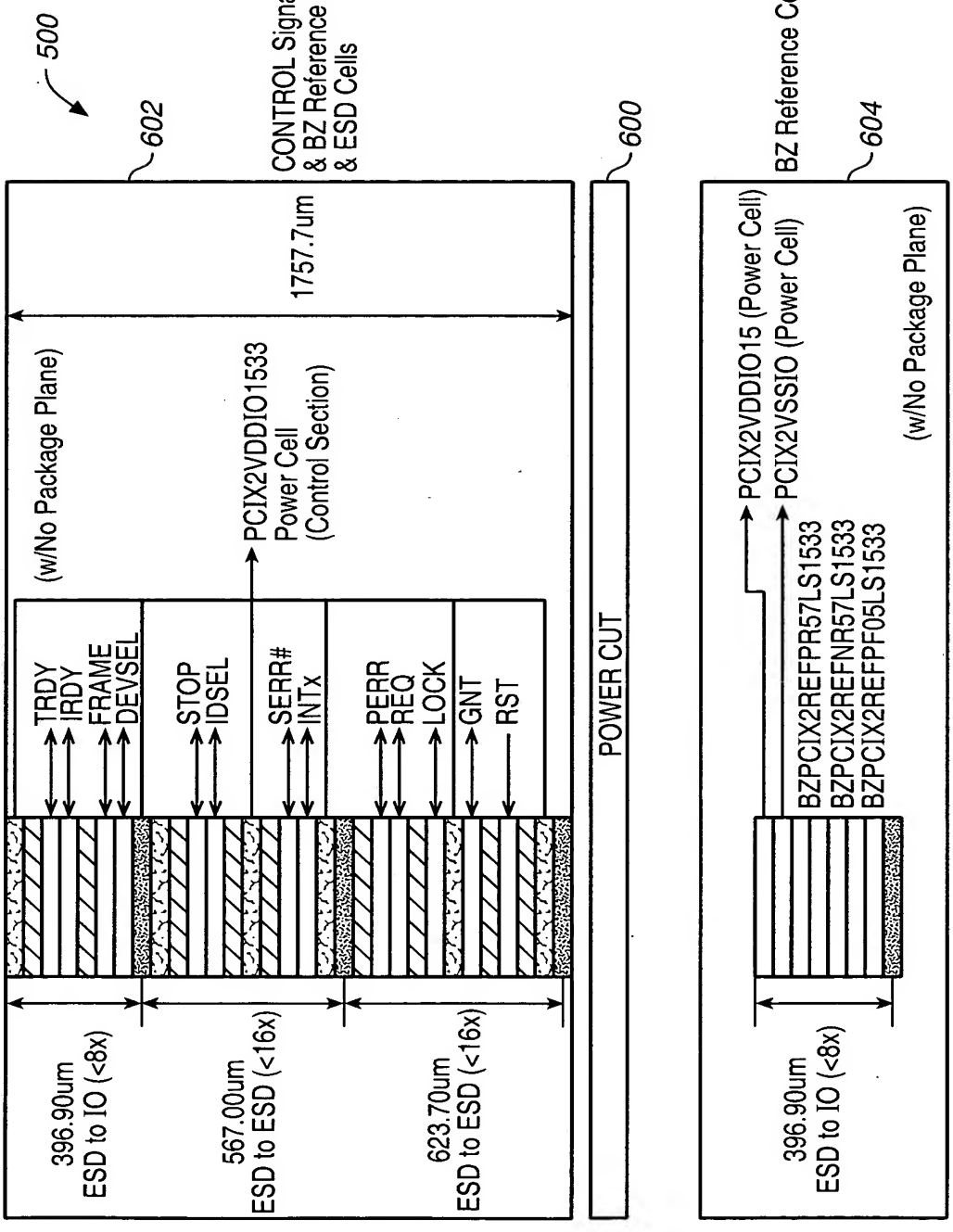

500
602
CONTROL Signals
& BZ Reference Cells
& ESD Cells
1757.7um
(w/No Package Plane)
PCIX2VDDIO1533
Power Cell
(Control Section)
TRDY
IRDY
FRAME
DEVSEL
STOP
IDSEL
SERR#
INTx
PERR
REQ
LOCK
GNT
RST
396.90um
ESD to IO (<8x)
567.00um
ESD to ESD (<16x)
623.70um
ESD to ESD (<16x)
600
POWER CUT
BZ Reference Cells
604
PCIX2VDDIO15 (Power Cell)
PCIX2VSSIO (Power Cell)
BZPCIX2REFPR57LS1533
BZPCIX2REFNR57LS1533
BZPCIX2REFPF05LS1533
(w/No Package Plane)
396.90um
ESD to IO (<8x)

FIG._8B

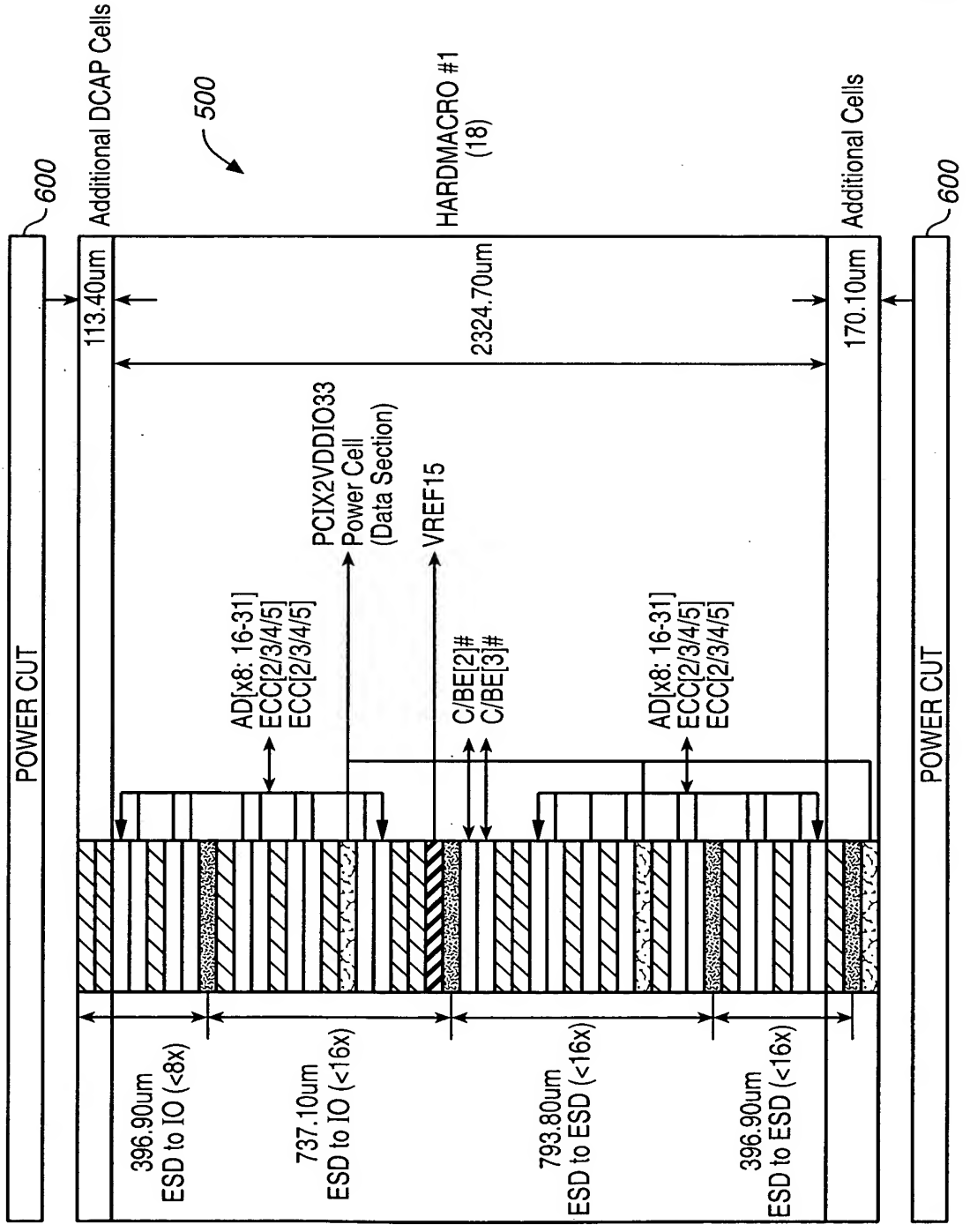

600
POWER CUT
Additional DCAP Cells
113.40um
500
HARDMACRO #1
(18)
2324.70um
Additional Cells
170.10um
600
POWER CUT
AD[x8: 16-31]
ECC[2/3/4/5]
ECC[2/3/4/5]
PCIX2VDDIO33
Power Cell
(Data Section)
VREF15
C/BE[2]#
C/BE[3]#
AD[x8: 16-31]
ECC[2/3/4/5]
ECC[2/3/4/5]
396.90um
ESD to IO (<8x)
737.10um
ESD to IO (<16x)
793.80um
ESD to ESD (<16x)
396.90um
ESD to ESD (<16x)

FIG._8C

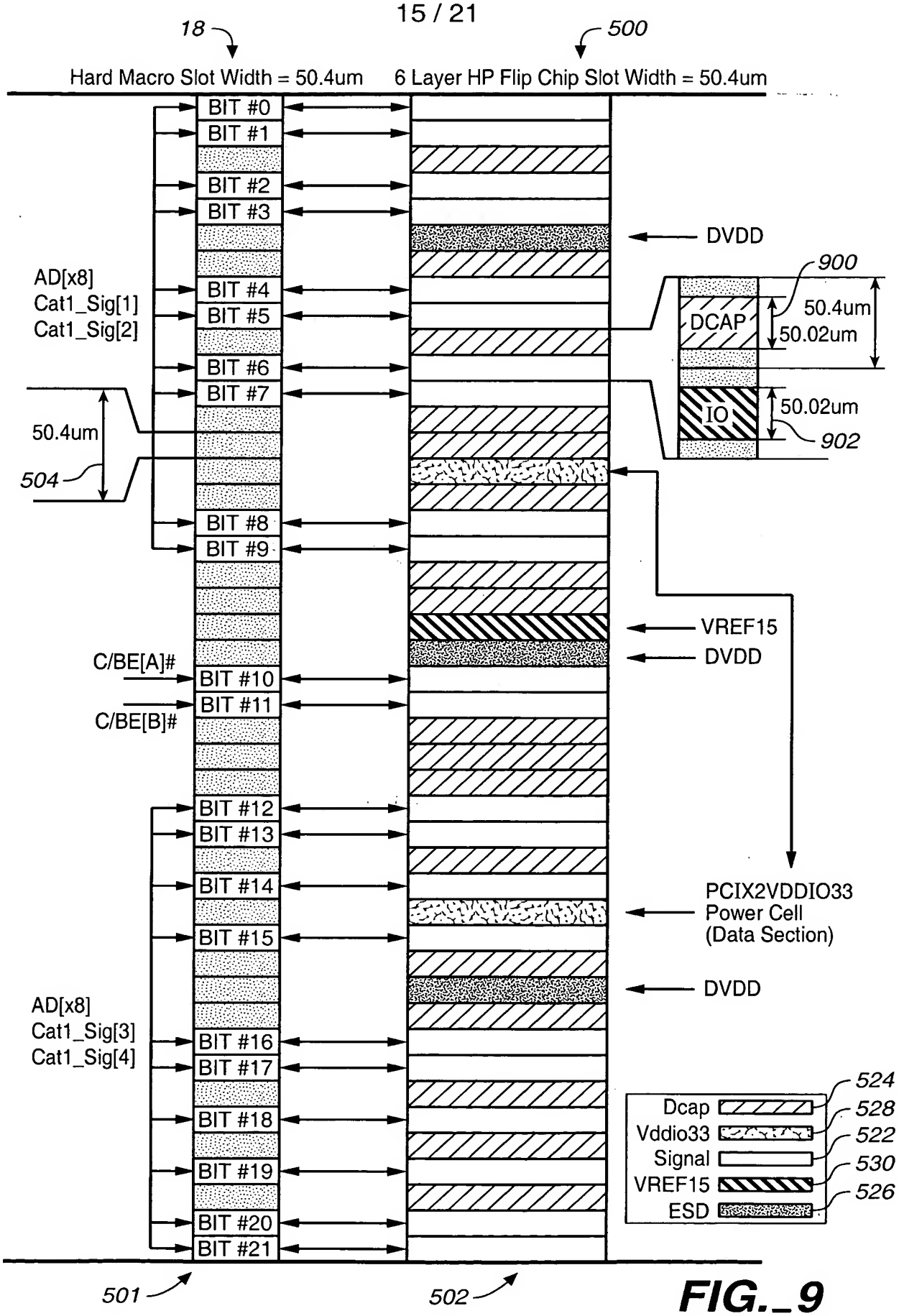

18
500
Hard Macro Slot Width = 50.4um
6 Layer HP Flip Chip Slot Width = 50.4um
BIT #0
BIT #1
BIT #2
BIT #3
BIT #4
BIT #5
BIT #6
BIT #7
BIT #8
BIT #9
BIT #10
BIT #11
BIT #12
BIT #13
BIT #14
BIT #15
BIT #16
BIT #17
BIT #18
BIT #19
BIT #20
BIT #21
AD[x8]
Cat1_Sig[1]
Cat1_Sig[2]
50.4um
504
C/BE[A]#
C/BE[B]#
AD[x8]
Cat1_Sig[3]
Cat1_Sig[4]
DVDD
900
DCAP
50.4um
50.02um
IO
50.02um
902
VREF15
DVDD
PCIX2VDDIO33
Power Cell
(Data Section)
DVDD
Dcap
Vddio33
Signal
VREF15
ESD
524
528
522
530
526
501
502

FIG._9

FIG._10

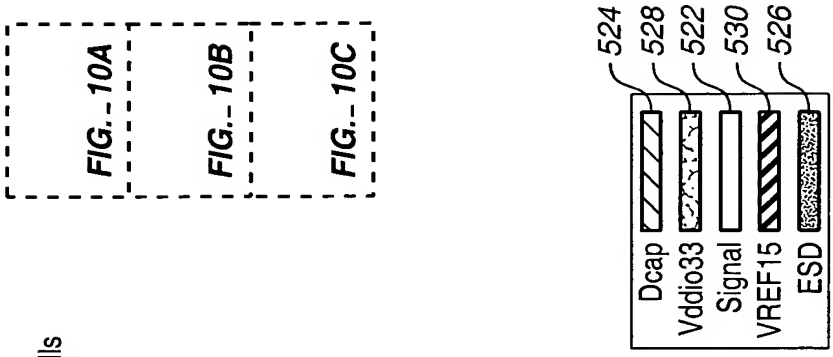
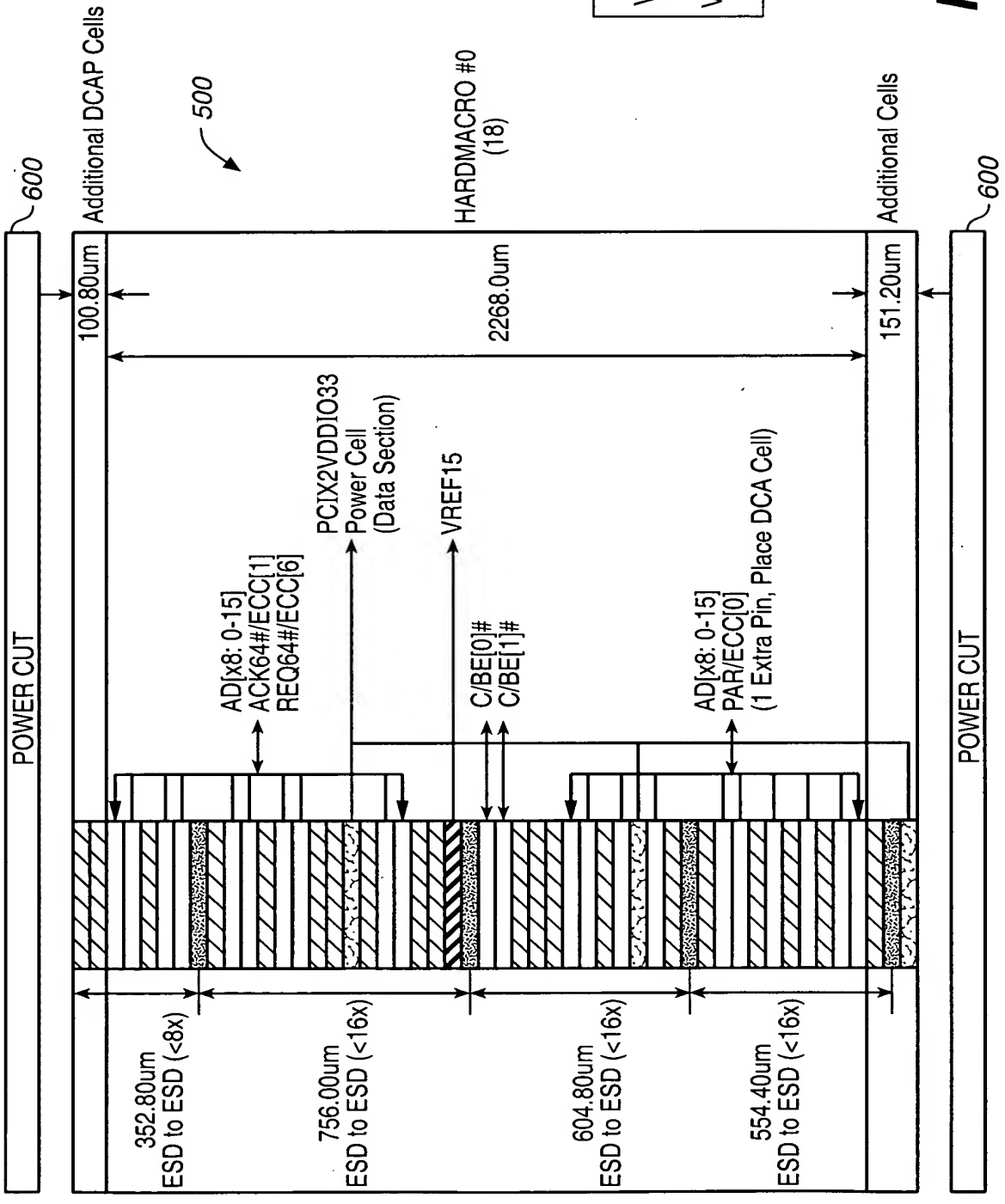


FIG._10A



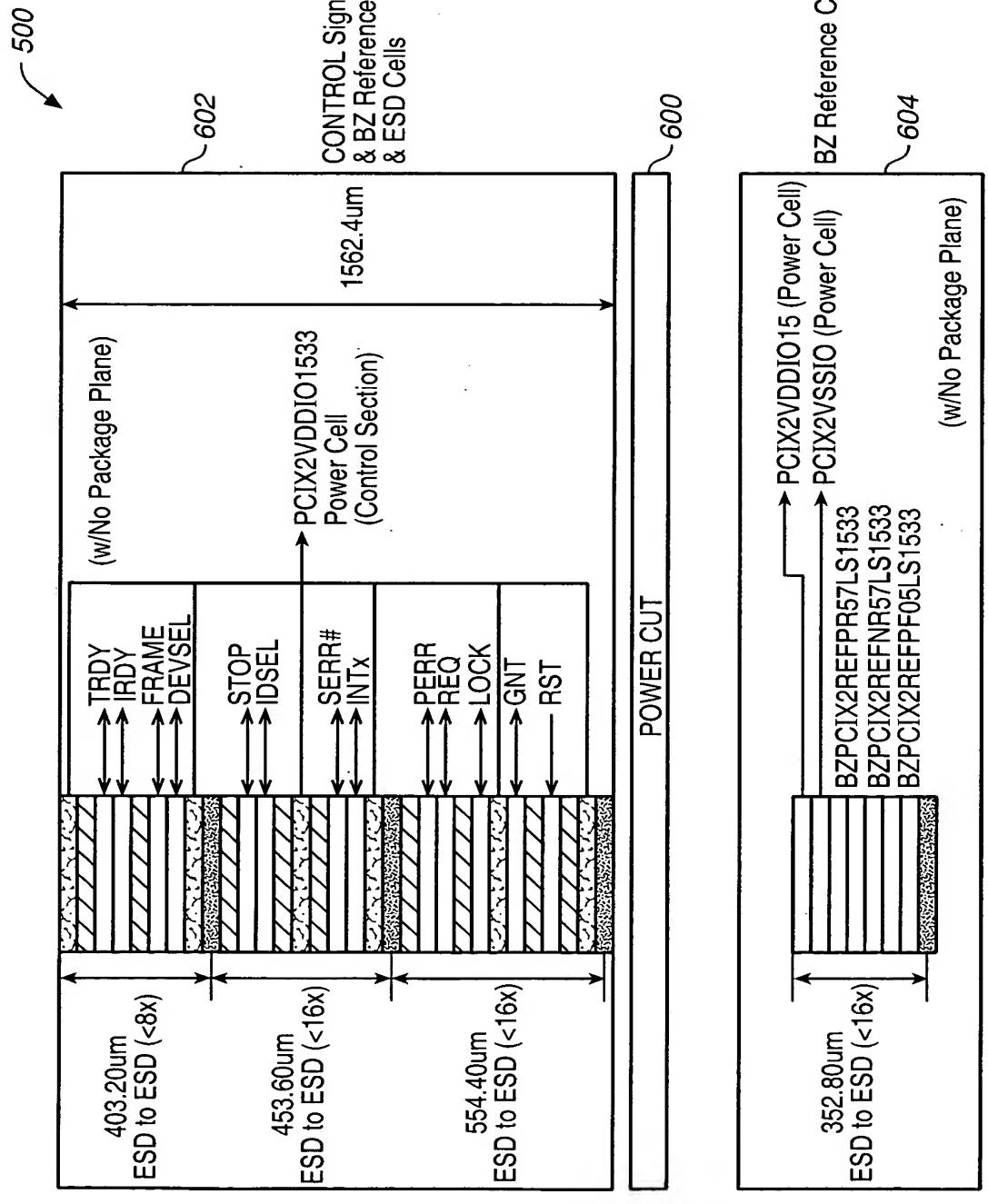

500
602
CONTROL Signals
& BZ Reference Cells
& ESD Cells
1562.4um
(w/No Package Plane)
PCIX2VDDIO1533
Power Cell
(Control Section)
TRDY
IRDY
FRAME
DEVSEL
STOP
IDSEL
SERR#
INTx
PERR
REQ
LOCK
GNT
RST
403.20um
ESD to ESD (<8x)
453.60um
ESD to ESD (<16x)
554.40um
ESD to ESD (<16x)
600
POWER CUT
604
BZ Reference Cells
PCIX2VDDIO15 (Power Cell)
PCIX2VSSIO (Power Cell)
BZPCIX2REFPR57LS1533
BZPCIX2REFNR57LS1533
BZPCIX2REFPF05LS1533
(w/No Package Plane)
352.80um
ESD to ESD (<16x)

FIG._10B

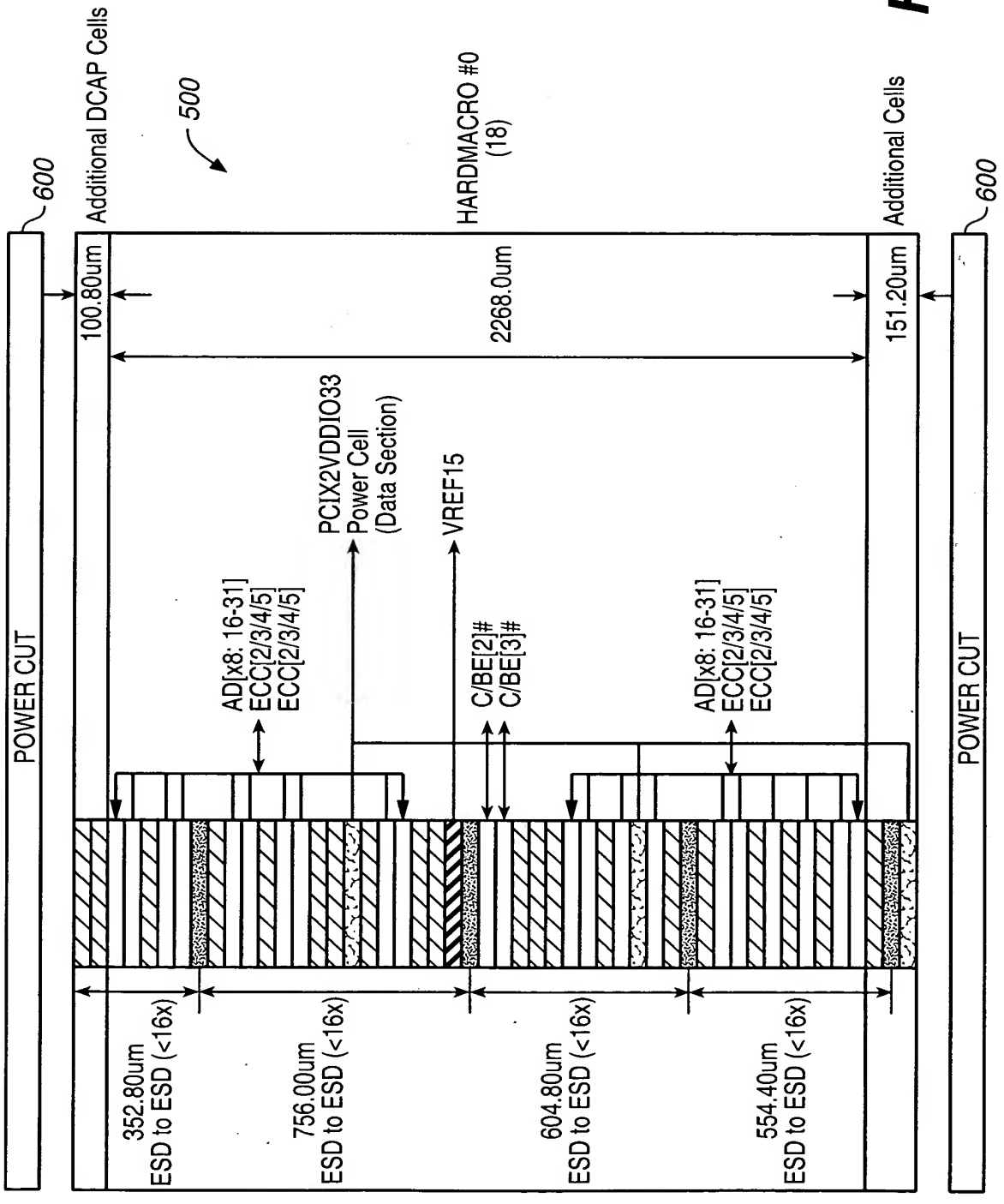

600
Additional DCAP Cells
500
HARDMACRO #0
(18)
Additional Cells
600
POWER CUT
100.80um
2268.0um
151.20um
POWER CUT
PCIX2VDDIO33
Power Cell
(Data Section)
VREF15
AD[x8: 16-31]
ECC[2/3/4/5]
ECC[2/3/4/5]
C/BE[2]#
C/BE[3]#
AD[x8: 16-31]
ECC[2/3/4/5]
ECC[2/3/4/5]
352.80um
ESD to ESD (<16x)
756.00um
ESD to ESD (<16x)
604.80um
ESD to ESD (<16x)
554.40um
ESD to ESD (<16x)

FIG._10C

Data Path Instance Pin Locations

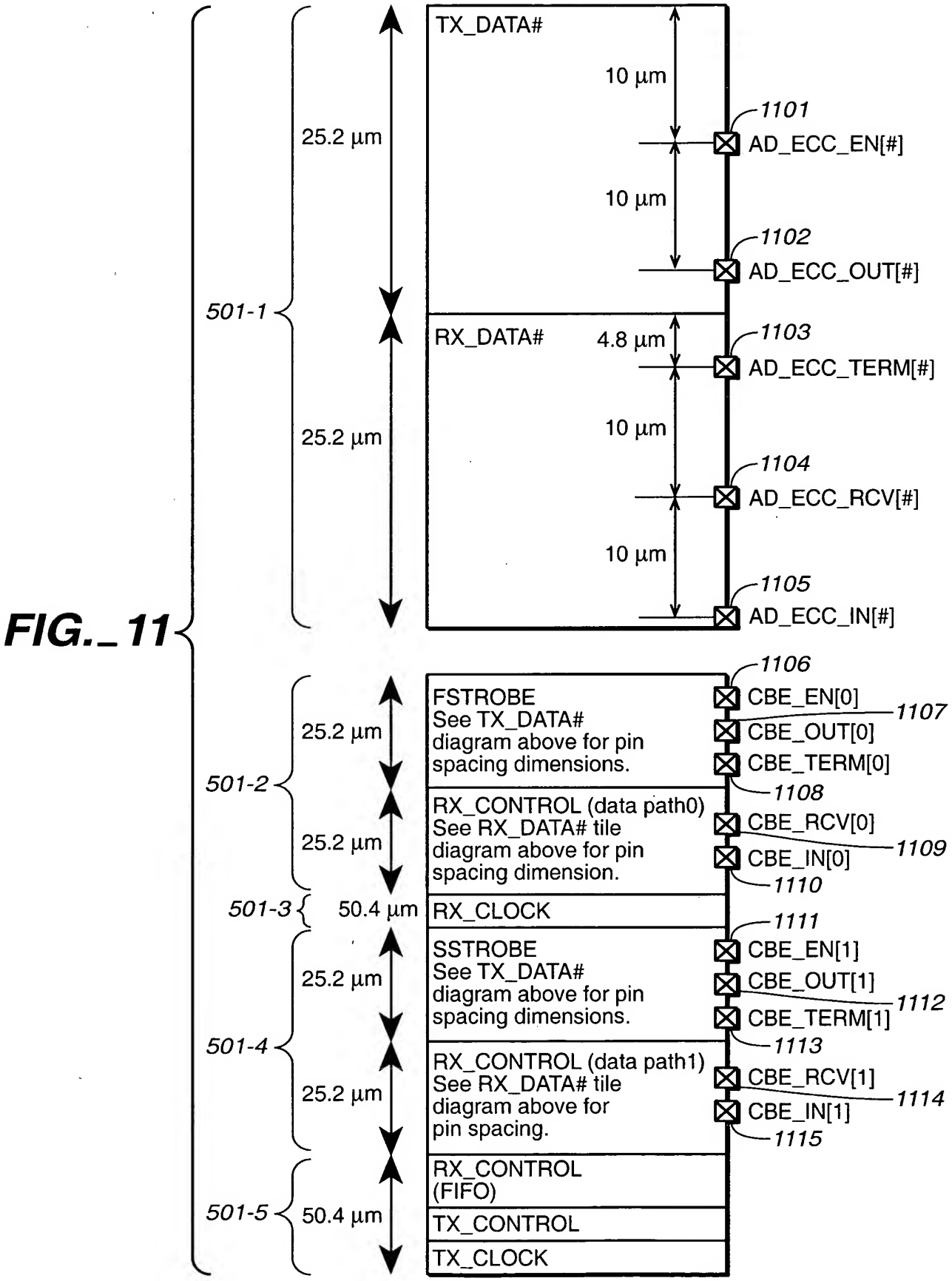


FIG._11

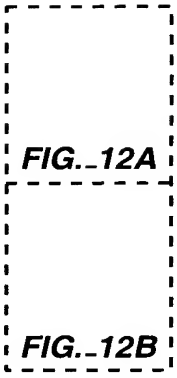
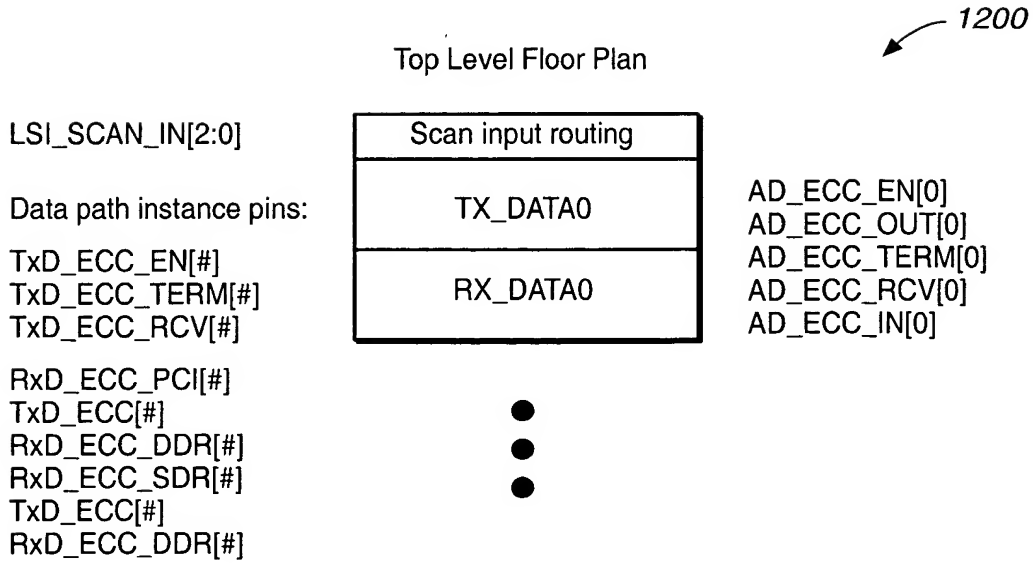


FIG._12

FIG._12A



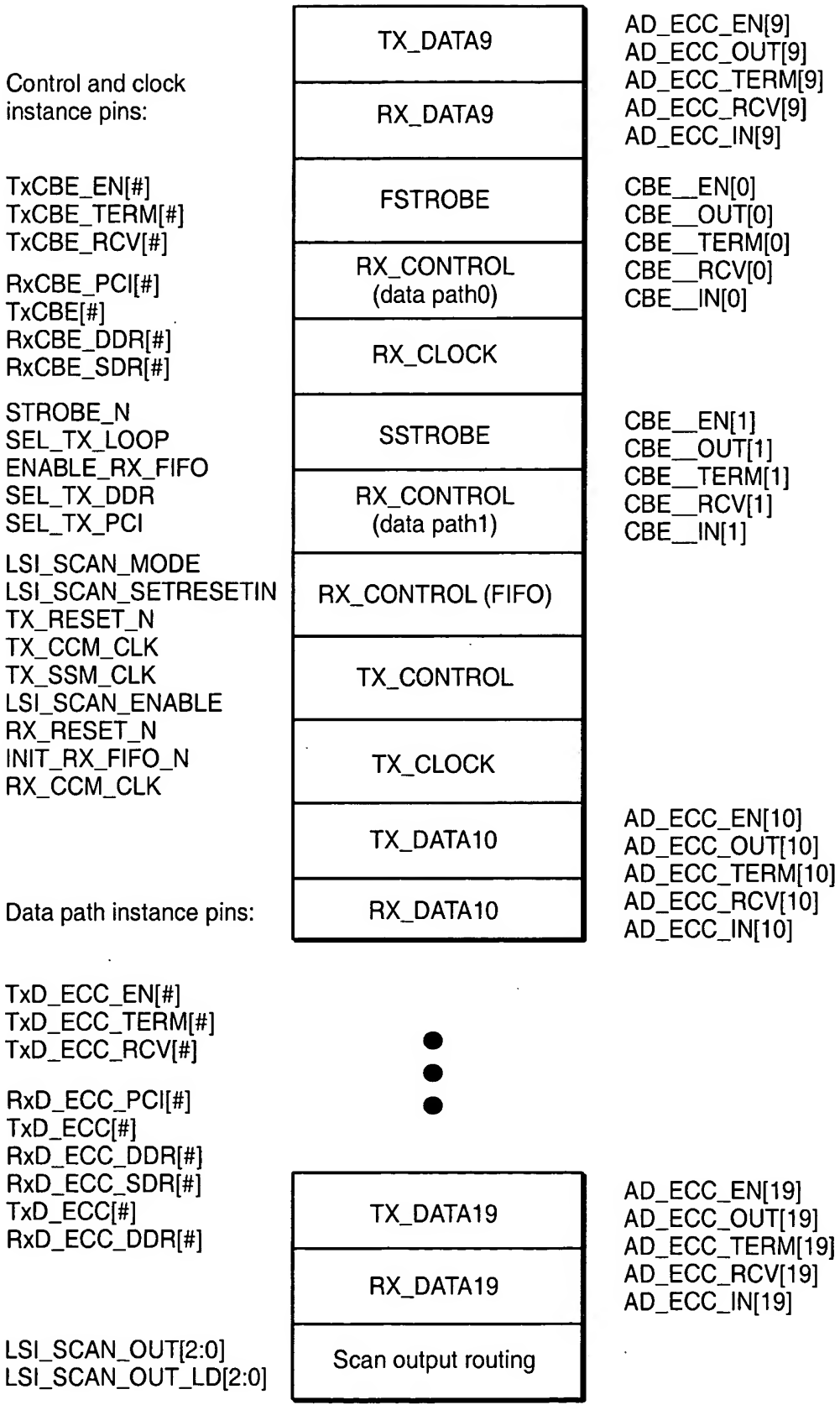

Control and clock instance pins:
TxCBE_EN[#]
TxCBE_TERM[#]
TxCBE_RCV[#]
RxCBE_PCI[#]
TxCBE[#]
RxCBE_DDR[#]
RxCBE_SDR[#]
STROBE_N
SEL_TX_LOOP
ENABLE_RX_FIFO
SEL_TX_DDR
SEL_TX_PCI
LSI_SCAN_MODE
LSI_SCAN_SETRESETIN
TX_RESET_N
TX_CCM_CLK
TX_SSM_CLK
LSI_SCAN_ENABLE
RX_RESET_N
INIT_RX_FIFO_N
RX_CCM_CLK
Data path instance pins:
TxD_ECC_EN[#]
TxD_ECC_TERM[#]
TxD_ECC_RCV[#]
RxD_ECC_PCI[#]
TxD_ECC[#]
RxD_ECC_DDR[#]
RxD_ECC_SDR[#]
TxD_ECC[#]
RxD_ECC_DDR[#]
LSI_SCAN_OUT[2:0]
LSI_SCAN_OUT_LD[2:0]
TX_DATA9
RX_DATA9
FSTROBE
RX_CONTROL (data path0)
RX_CLOCK
SSTROBE
RX_CONTROL (data path1)
RX_CONTROL (FIFO)
TX_CONTROL
TX_CLOCK
TX_DATA10
RX_DATA10
TX_DATA19
RX_DATA19
Scan output routing
AD_ECC_EN[9]
AD_ECC_OUT[9]
AD_ECC_TERM[9]
AD_ECC_RCV[9]
AD_ECC_IN[9]
CBE__EN[0]
CBE__OUT[0]
CBE__TERM[0]
CBE__RCV[0]
CBE__IN[0]
CBE__EN[1]
CBE__OUT[1]
CBE__TERM[1]
CBE__RCV[1]
CBE__IN[1]
AD_ECC_EN[10]
AD_ECC_OUT[10]
AD_ECC_TERM[10]
AD_ECC_RCV[10]
AD_ECC_IN[10]
AD_ECC_EN[19]
AD_ECC_OUT[19]
AD_ECC_TERM[19]
AD_ECC_RCV[19]
AD_ECC_IN[19]

FIG._12B